ABSTRACT OF THE DISCLOSURE

The present invention provides an ESD protection component, comprising at least two MOS field effect transistors (FETs) of a first conductivity type and a first well having a first conductivity type. The two MOS FETs have two parallel gates formed on a first semiconductive layer having a second conductivity type. The first well formed on the first semiconductive layer is comprised of a connecting area formed between the MOS FETs, two parallel extension areas formed perpendicular to the gates of the MOS FETs, and a first doping area of the second conductivity type formed in the connecting area. Two SCR are formed with drains of the MOS FETs, the first semiconductive layer, the first well and the first doping region. With the combination of the SCR and NMOS FET, ESD protection efficiency can be substantially enhanced.